REMARKS

At page 2 of the Office Action, the Examiner rejects claims 1 and 7 under 35 U.S.C. §103(a) as being unpatentable over Cyman et al. (US Patent No. 5,949,438). Reconsideration and withdrawal of this rejection is respectfully requested in light of the following comments.

Obviousness can only be established by combining or modifying teachings of the prior art to produce the claimed invention where there is teaching, suggestion or motivation to do so found either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art.

Cyman et al. is directed to a raster image processing system that generates images from input representations with sufficient speed that printing can occur substantially in the same real-time as raster image processing of the input data. Cyman et al. discloses that different print engine control modules 600 can be replaceably plugged into and out of the system to facilitate use with different types of print engines 68. However, Cyman et al. highlights and propagates the problem not previously recognised in the prior art which the present invention addresses. Cyman et al. teaches away from the solution provided by the presently claimed invention and provides no motivation for one of ordinary skill in the art to arrive at the invention of claim 1.

Cyman et al. is directed to high speed, high resolution, intelligent electronic imaging, and more particularly to high speed electronic plateless printing (col. 1, lines 9-11). Such systems are relatively complex and have low consumer turnover rates of equipment. As discussed in the "Background of the Invention" section of the present specification, prior art systems, such as that disclosed in Cyman et al., include standard components that are capable of being programmed to carry out specific tasks. This permits manufacturers to avoid the necessity of having to fabricate task-specific microcontrollers or microprocessors. It is counter-intuitive to have, and Cyman et al. expressly teaches away from, a microcontroller that incorporates print head interface circuitry provided on a wafer substrate together with processor circuitry. Cyman et al. specifically teaches that different engine control modules 600 can be used depending on the particular print engine 68 being employed. To use raster image processor 64 with a different print engine 68, a technician can unplug one engine control module 600, embodied as a modular printed circuit board, from a back plane connecting it to the rest of raster image

processor 64, and plug in another engine control module 600 designed for the new print engine (col. 16, line 67-col. 17, line 6).

This is in sharply evident contrast to the present invention as claimed in either claim 1 or claim 7, wherein processor circuitry is provided on a wafer substrate which also includes print head interface circuitry on the wafer substrate, in addition to bus interface circuitry. The Examiner considers that it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the processor circuity and print head interface circuitry on a single wafer substrate. It is respectfully submitted that in light of the foregoing clarification, this is not the case. One of ordinary skill in the art is evidently taught, as evidenced by Cyman et al., to provide the engine control module 600 on an interchangeable printed circuit board to allow interconnectivity with a variety of print engines 68. There is no motivation or suggestion in the prior are relied upon, or in the knowledge generally available to one of ordinary skill in the art, to teach one of ordinary skill in the art to manufacture a microcontroller that comprises both processor circuitry and printhead interface circuitry on a wafer substrate.

At pages 2-3 of the Office Action, the Examiner rejects claim 2 under 35 U.S.C. §103(a) as being unpatentable over Cyman et al. in view of Granzow (US Patent No. 5,751,318). Reconsideration and withdrawal of this rejection is respectfully requested in light of the following comments.

The preceding comments for claim 1 equally apply for independent claim 2. That is, there is no motivation or suggestion to one of ordinary skill in the art that it would beneficial to provide a microcontroller that comprises both the processor circuitry and print head interface circuitry on a common wafer substrate. Granzow would not motivate one of ordinary skill in the art to arrive at the invention claimed in claim 2.

Furthermore, it is respectfully submitted that it would not have been obvious to include print head interface circuitry as an integral part of a microcontroller that controls a page width printhead having a nozzle arrangement defining a microelectromechanical device that is capable of being actuated to eject ink from a nozzle chamber of the nozzle arrangement. Although Granzow discloses an inkjet printhead, Granzow contributes nothing to any prior teaching of a microcontroller as claimed in claim 2 of the present application.

At pages 3-4 of the Office Action, the Examiner rejects claim 4 under 35 U.S.C. §103(a) as being unpatentable over Cyman in view f Granzow and in further view of Lloyd (EP A 0334546). Reconsideration and withdrawal of this rejection is respectfully requested in light of the following comments.

The pulse generator 13 should not be construed as print head interface circuitry as used in present claim 4. Print head interface circuitry is positioned on a wafer substrate and is connected between processor circuitry and the print head, the print head interface circuitry being configured to facilitate communication between the processor circuitry and the print head. It is respectfully submitted that pulse generator 13 does not act as print head interface circuitry that defines a number of registers for storing clocking and control information to be received by the print head in accordance with a predetermined algorithm. Pulse controller 19 transfers values to pulse generator 13 while triggering one or more pulses per parameter value. Pulse controller 19 converts the program information it receives from test generator 23 into control signals which are transmitted from its pulse parameter value output port PPV along bus 33 to pulse delay D, pulse width W and pulse amplitude A input ports of the pulse generator 13. The pulse generator 13 produces rectangular pulses whose energy is controlled by varying pulse width and/or pulse voltage amplitude (col. 6, line 13-37). It is respectfully submitted that this does not disclose registers in the pulse generator 13 able to store clocking and control information in accordance with a predetermined algorithm as required in the claim.

At page 4 of the Office Action, the Examiner rejects claims 5 and 6 under 35 U.S.C. §103(a) as being unpatentable over Cyman et al. in view of Granzow and Lloyd, and in further view of Kupcho et al. (US Patent No. 5,670,995). Reconsideration and withdrawal of this rejection is respectfully requested in light of the following comments.

The Examiner considers print head interface circuitry to be disclosed by Printer CPU 216 in Kupcho et al., which is connected to the data bus and the CPU of a computer system. However, claims 5 and 6 of the present application ultimately depend from claim 2 which requires the print head interface circuitry to be connected between processor circuitry and a print head, the print head interface circuitry being configured to facilitate communication between the processor circuitry and the print

head. Discrete bus interface circuitry is connected to the processor circuitry that is discrete to the print head interface circuitry. The central processing unit, not being the aforementioned processor circuitry, is connected to the print head interface circuitry, in conjunction with the requirements concerning the aforementioned separate processor circuitry. It is respectfully submitted that such an arrangement is not disclosed in Kupcho et al. where the Printer CPU 216 is simply connected to a computer system CPU via a data bus.

Moreover, referring to present claim 6, the memory buffers 218 and 220 of Fig. 5 in Kupcho et al. are not connected to both the print head interface circuitry and the processor circuitry. It is respectfully submitted that it is clear that the Printer CPU 216 in Kupcho et al. is not configured to receive a print image from the processor circuitry via the memory buffers 218 or 220, as is required in present claim 6.

CONCLUSION

In view of the foregoing, it is respectfully requested that the Examiner reconsider and withdraw the rejections under 35 U.S.C. §103(a). The present application is believed to be in condition for allowance. Accordingly, the Applicant respectfully requests a Notice of Allowance of all the claims presently under examination without amendment.

Very respectfully,

Applicant:

KIA SILVERBROOK

C/o: Silverbrook Research Pty Ltd
393 Darling Street
Balmain NSW 2041, Australia

Email: Kia.silverbrook@silverbrookresearch.com

Telephone: +612 9818 6633

Facsimile: +61 2 9818 6711